Figure 16 is an eye diagram of the laser output given the asymmetric driver pulse of Figure 15 in accordance with one embodiment of the present invention.

Figure 17 is a graph of the chirp resulting from the driver pulse of Figure 15 in accordance with one embodiment of the present invention.

Figure 18 is an eye diagram of pulse propagation over single mode optical fiber in accordance with one embodiment of the present invention.

Figure 19 is a graph of bit-error showing the error associated with symmetric driver pulses and asymmetric driver pulses in accordance with one embodiment of the present invention.

Figure 20 is a set of graphs of a symmetric pulse driver output, transmitter output, received signal and filtered signal.

Figure 21 is a set of graphs of an asymmetric pulse driver output, transmitter output, received signal and filtered signal in accordance with one embodiment of the present invention.

Figure 22 is a graph of sensitivity contours in accordance with one embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention provide for ringing and inter-symbol interference reduction in optical communications. In the following description, numerous specific details are set forth to provide a more thorough description of embodiments of the invention. It is apparent, however, to one skilled in the art, that the invention may be practiced without these specific details. In other instances, well known features have not been described in detail so as not to obscure the invention.

In one embodiment of the present invention, the rise time of the signal is longer than the fall time of the signal. The resulting asymmetrical driver pulse is sent to the laser. The resulting overshoot, ringing, undershoot and chirp of the output from the laser are greatly reduced, resulting in better receiver sensitivity. The eye of the signal is approximately symmetrical and is less closed.

Figure 8A illustrates a driver output where the rise time is longer than the fall time. The rise time 802 is the distance in time between when the pulse is initiated at 0 and when the pulse rises to its high value of 1. The fall time 804 is the distance in time between when the pulse begins to fall from its high value of 1 and when it reaches its low value of 0.

In various embodiment, the rise time is at least 50% longer than the fall time. In other embodiments, the rise time is at least twice the fall time. In still other embodiments, the rise time is at least 30% of the bit-period.

Figure 8B illustrates the use of a pulse shaper in a transmitter in accordance with the present invention. A pulse shaper 800 connects to a rise time control signal 820. An input pulse 810 is provided to the pulse shaper. The rise time control signal is used to increase the

rise time of the incoming pulses. Once the pulse rise time is adjusted, the signal is sent to a laser 830.

Figure 8C illustrates the process of shaping a driver pulse in accordance with one embodiment of the present invention. At step 850, the input signal is generated. At step 870, the rise time of each pulse in the signal is increased. At step 880, the modified signal is sent to the laser.

Duty Cycle Distorter

In one embodiment, a series of duty cycle distorters are used to increase pulse rise time. Figure 9 illustrates a duty cycle distorter in accordance with one embodiment of the present invention. The positive supply voltage, $V_{cc}$, couples to resistor R1, resistor R2, resistor R3, resistor R4, the collector of transistor M1 and the collector of transistor M2. Resistor R1 couples to the base of transistor M1, the collector of transistor M3 and resistor R5. Resistor R2 couples to the base of transistor M2, the collector of transistor M4 and resistor R6.

The emitter of transistor M1 couples to resistor R7 and the base of transistor M5. The emitter of transistor M2 coupled to resistor R8 and the base of transistor M6. Resistor R3 couples to signal OUT+ and the collector of transistor M5. Resistor R4 couples to signal OUT- and the collector of transistor M6. The IN+ signal couples to the base of transistor M3. The IN- signal couples to the base of transistor M4.

The negative supply voltage, $V_{ee}$, couples to current generator $I_1$, current generator $I_-$, current generator $I_+$, current generator $I_2$, resistor R7 and resistor R8. Current generator $I_1$ couples to the emitters of transistor M3 and transistor M4. Current generator $I_-$ couples to